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41 Min-Delay: Pulsed Latches $T_{t} T_{Tcd} C_{cq} P_{w} \geq - + hold$

$CL Q1 D2 Q1 D2 \phi P T Pw \phi P L1 \phi P L2 T Cd T Hold T$

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Figure 6. Verilog Netlist Options. Remove Behavioral

And Functional From The View List (this Has To Do

With The Hierarchical Levels That Are Descended 2th,

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