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Into One Circuit With One Common Binary Adder. This Is Done By Including An Exclusive-OR Gate With Each Full Adder. A 4-bit Adder-subtractor Circuit Is Shown In Figure 2. Input S Controls The Operation. 1. When $S = 0$ The Circuit Is An Adder. 2. When $S = 1$ The Circuit Becomes A Subtractor. May 3th, 2024
Nuclei FPGA Evaluation Boards And Debugger Kit Introduction
Prototype The Nuclei Evaluation SoC (included RISC-V Core) In FPGA Boards; And The Nuclei Made JTAG Debugger Kit (called Hummingbird Debugger Kit), Which Can Be Used To Debug The RISC-V Core In FPGA Prototype Or In Real Chip. Figure 1-1 Jun 2th, 2024.

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