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1 (TRUE) Is Converted To A Logic State 0 (FALSE) Or Vice Versa [IEC 60617-12, IEC  
61082-2] 3.20 Logic Inversion Condition Mainly Used With Binary Logic Elements  
Where A Higher Physical Level Is Converted To A Lower Physical Level Or Vice Versa  
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Requires Single Phase Clock With 33% Duty Cycle To Provide Internal Timing. • 8086 Is Designed To Operate In Two Modes, Minimum And Maximum. • I Mar 3th, 2024  
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