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Using ModelSim To Simulate Logic Circuits For Altera FPGA ... Figure 3. Verilog Code For The Top-level Module Of The Serial Adder. The Verilog Code For The FSM Is Shown In Figure 4. The FSM Is A 3-state Mealy finite State Machine, Where The first And The Third State Waits For The Start Input To Be Set To 1 Or 0, Respectively. The Computation Of The Sum Of A And B 4 Altera Corporation - University Program January 2011 3th, 2024 Writing A Testbench In Verilog & Using Modelsim To Test 1 ... With More Complicated Designs. The Purpose Of This Lab Is To Get You Familiarized With Testbench Writing Techniques, Which Ultimately Help You Verify Your Final Project Design Efficiently And Effectively. You Will Also Learn Scripting DO Files To Control Simulation In Modelsim And To Facilitate Quick Repeated Simulations During Debugging. 2. 3th, 2024 Modelsim Manual ModelSim Reference Manual - Georgia Institute Of Technology ModelSim SE User's Manual ModelSim /VHDL, ModelSim /VLOG, ModelSim /LNL, And ModelSim /PLUS Are Produced By Model Technology™ Incorporated. Unauthorized Copying, Duplication, Or Other Reproduction Is Prohibited Without The Written Consent Of Model Technology.

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Page 4 2. Specify EDA Tool Settings On Page 4 3.
Launch Simulation From The Intel Quartus Prime
Software On Page 6 1th, 2024.

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Output. Figure 6. ModelSim Simulator Wave 1th,
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